Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

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**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GATE**

**Process: 53**

**APPROVED BY: DK DIE SIZE .013” X .018” DATE: 10/6/21**

**MFG: FAIRCHILD THICKNESS .009” P/N: 2N4117A**

**DG 10.1.2**

#### Rev B, 7/19/02